Discrepant ESD-CDM Test System and Failure Yield Prediction between ESD Association and JEDEC Standards

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Abstract: CDM test system and verification method of ESDA and JEDEC standards have been studied. There are several different items. They can be categorized into 5 major items, which are charging system, discharging system, verification module, waveform verification, and classification level. Regarding waveform verifications at each stress level, ESDA system provides higher peak current whereas lower rise time and lower full width at half maximum, compared to JEDEC system. It implies that ESDA standard provides higher inductance in a discharge system and higher discharge energy, which make it more severe system. The current continuously increases with the stress level. The linear relationship of stress conditions by these standards can be obviously observed. The electrical failure yield of each standard system is then predicted by a stress condition of the other system.

Keywords: ESD, CDM, ESDA, JEDEC, Electrical failure yield

1 INTRODUCTION

Along with the development of technology, modern electronic systems become largely integrated, so they have become more and more sensitive to electrostatic discharge (ESD). This phenomenon has turned to be a serious problem for IC products fabricated by deep-submicron CMOS technology although design effort and awareness are significantly improved [1-3]. It impacts the functionality, reliability and lifetime of ICs [4]. Therefore, EOS/ESD test is required to qualify products based on customer expectations to minimize failures due to ESD from human and mechanical handling.

ESD events have been divided into 4 models, which are Human Body Model (HBM), Machine Model (MM), Charge Device Model (CDM), and Socket Device Model (SDM). Regarding the increase of automated component handling systems, CDM becomes a significantly test for microelectronic components. It is performed to classify the susceptibility of a device to determine its ESD withstand voltage to such ESD events. This CDM test simulates that the device itself becomes charge and is rapidly discharged when it approaches a conductive object. The rapid transfer of an electrical charge causes most of the ESD damages in the electronic manufacturing.

To predict and qualify the ESD immunity level, there are several organizations that make the ESD related primary standards. They are Electrostatic Discharge Association (ESDA), Automotive Electronics Council (AEC), Electronic Industries Alliance/Joint Electron Device Engineering Council (EIA/JEDEC) and US Military Standard (MIL-STD). The commonly used standards are released by ESDA and JEDEC. They have made their own definitive stipulations on test methods and instruments. With the different specification, some unavoidable questions, such as the similarity of the test system verification, occur. In this paper, we present the discrepant detail of CDM test between ESDA and JEDEC including their correlative stress condition and prediction of the electrical failure yield.

2 DISCREPANT ESD-CDM TEST SYSTEM BETWEEN ESDA AND JEDEC STANDARDS

An ESD-CDM event is characterized by the rapid transfer of an electrical charge from an ESD sensitivity device to a metallic body with different electrostatic potential. A device may acquire a potential during the manufacturing processes either through direct contact, which typically takes place when it slides down a tube or along the surface of a loader or through induction of an electrostatic field in its environment, and discharge through contact with a grounded surface.

The equipment for this test consists of an ESD pulse simulator and digital phosphor oscilloscope. The charged-up device is then discharged through the discharge plate and the discharge waveform is captured by a large-bandwidth oscilloscope. The performance of the simulator can be dramatically degraded by parasitic components in the discharge path. Therefore, the waveform performance is verified using the standard verification module to ensure proper simulation and repeatable ESD results. The waveform verification shall be performed prior to performing CDM testing. If the waveforms do not meet the requirements, the testing shall be halted until waveforms are compliant.

Regarding the reference of ESDA and JEDEC standards, there are several non-identical aspects about the experimental methods and instruments, which can cause different verification results. It can be distributed into 5 major items, which consist of charging system, discharging system, verification module, classification level, and waveform verification. The first 4 items and the last one are shown in Table 1 and Table 2, respectively. From the table, we can see that there are several different details including the

verification module and oscilloscope bandwidth, which are the major factors on the system verification. Furthermore, the different of the equipment capability affords the different results since CDM test is a very fast incident. All of these could effect to the different verification waveforms, implying the test results. To compare further the performance of these two standards, the relationship of the stress condition between ESDA and JEDEC standards is unavoidable to investigate through the discharge energy and the peak current.

Table 1 The Difference between JEDEC and ESDA in Charging system, Discharging system, Verification module, and Classification level

Item	JEDEC [5]	ESDA [6]
1. Charging system - Charging electrode size - Charging resistor - Dielectric type/thickness	 - Larger than the size of the component - 300 MΩ - FR-4/0.381±0.038 mm (0.015±0.0015 in)	 - At least 7 times larger in area than the size of the component - At least 100 MΩ - No detail/≤130 μm
2. Discharging system - Ground plane - Probe - Oscilloscope	 - Square conductive plate with edge length of 63.5±6.35 mm (2.5±0.25 in) - At least 3 GHz bandwidth - 1 GHz bandwidth	 - No detail - At least 5 GHz bandwidth - 1 or 3.5 GHz bandwidth
3. Verification module material/Thickness - Small module capacitance at 1 MHz /Diameter - Large module capacitance at 1 MHz /Diameter	Brass plated with nickel or gold/nickel and optionally have a gold flash coating over the nickel/Thickness: 1.27±0.05 mm (0.050±0.002 in) - 6.8±5% pF/8.89±0.127 mm (0.35±0.005 in) - 55±5% pF/25.4±0.127 mm (1.000±0.005 in)	Two gold plated or nickel-plated copper disks on single sided 0.8 mm thick FR-4 circuit board with the size at least 30x30 mm^2 - 4±5% pF/approximately 26 mm - 30±5% pF/approximately 9 mm
4.Classification level	4 classes Class: Voltage range I: <200 V II: 200 – 500 V III: 500 – 1000 V IV: ≥1000 V	7 classes Class: Voltage C1: <125 V C2: 125 – 250 V C3: 250 – 500 V C4: 500 – 1000 V C5: 1000–1500V C6: 1500-2000V C7: ≥2000 V

Table 2 ESDA and JEDEC waveform requirement at 1 and 3.5 GHz bandwidth

Standard	ESDA (1 GHz)				ESDA (3.5 GHz)				JEDEC (3GHz)			
Charge Voltage (± 5%)	I_{p1} (A) [4 pF± 5% at 1 MHz]		I_{p1} (A) [30 pF± 5% at 1 MHz]		I_{p1} (A) [4 pF± 5% at 1 MHz]		I_{p1} (A) [30 pF± 5% at 1 MHz]		I_{p1} (A) [6.8 pF± 5% at 1 MHz]		I_{p1} (A) [55 pF± 5% at 1 MHz]	
	min	max	min	max	min	max	min	max	min	max	min	max
125 V	0.904	1.356	NA	NA	1.520	2.280	NA	NA	NA	NA	NA	NA
250 V	1.800	2.700	NA	NA	3.000	4.500	NA	NA	NA	NA	NA	NA
500 V	3.600	5.400	11.200	16.800	6.000	9.000	14.400	21.600	4.888	6.613	9.775	13.225
1000 V	7.200	10.800	NA	NA	12.000	18.000	NA	NA	9.775	13.225	NA	NA
1500 V	10.800	16.200	NA	NA	18.000	27.000	NA	NA	NA	NA	NA	NA
2000 V	14.400	21.600	NA	NA	24.000	36.000	NA	NA	NA	NA	NA	NA
t_r (ps)	< 400		< 400		< 200		< 250		< 400		NA	NA
t_d (ps)	< 600		< 1000		< 400		< 700		500	1500	NA	NA
I_{p2} (A)	< 50% of I_{p1}		< 50% of I_{p1}		< 50% of I_{p1}		< 50% of I_{p1}		< 50% of I_{p1}		< 50% of I_{p1}	
I_{p3} (A)	< 25% of I_{p1}		< 25% of I_{p1}		< 25% of I_{p1}		< 25% of I_{p1}		< 25% of I_{p1}		< 25% of I_{p1}	

3 CORRELATION OF STRESS CONDITION

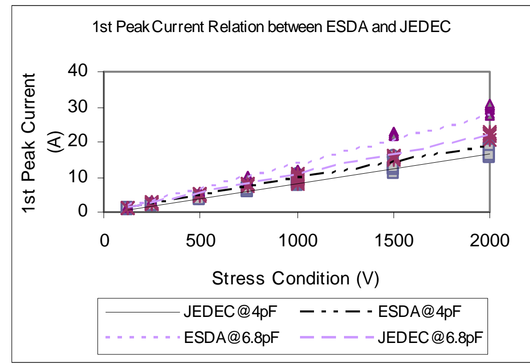
Since the CDM test system has to be ensured for the proper simulator and repeatable results, the waveform verification shall be performed using the verification module. It results in a discharge waveform. The discharge energy typically represents the capacitance of the test module. A larger capacitance provides more discharge energy. It is assumed that the stored energy in the module – nearly fully charged, which acts as the capacitor, can totally discharge. That refers the discharge energy should equal to the energy stored in the module. The CDM peak current during the verification can be measured to represent the discharge energy at each stress condition and the relation between the discharge energy and peak current can be shown in Equation (1). This implies that the discharge energy can be estimated by the square of the first CDM peak current.

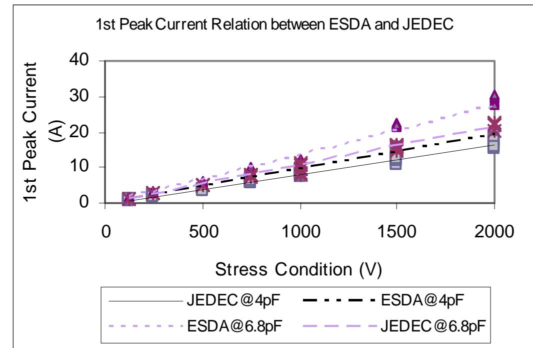
$$E_{\text{discharge}} \prec I_{p1}^2 \tag{1}$$

where, $E_{\text{discharge}}$: Discharge energy and I_{p1} : Discharge first peak current

With the relation of the discharge energy and the CDM peak current, we have varied the stress condition and verified the waveforms with 4 pF and 6.8 pF modules by ESDA and JEDEC discharge plates. The results clearly illustrate that I_{p1} of ESDA discharge system is higher than that of JEDEC as shown in Fig. 1 (a); however, the rise time (tr) and the full width at half maximum (td) show contrarily lower. These imply that the ESDA discharge plate makes more inductance to the discharge system, and then the system enters the steady state faster. It also supplies the higher discharge energy to the environment and behaves as the more severe test. In addition, the discharge energy causes certain influence to the electrical test yield. We can predict the consequence of each system by the other system through a relationship of discharge energy and peak current. Fig. 1 (b) shows the linear relationship of the ESDA and JEDEC stress conditions as expected. It may be noted that the ESDA test system provides the higher electrical failure yield because of its higher discharge energy at the same stress condition.

After we have performed CDM test on several units by these two systems, peak currents during test and stress voltages are compared. The electrical test is subsequently on process and its results infer a relation of electrical failure yields between these systems. The peak currents of discharge waveforms continuously increase with a stress voltage and so do the electrical failure yields. The relations among the peak current, electrical failure yield and stress voltage of a device AM29SL800DT/DB with TSOP048 and AM29BL802D with SSO056 are demonstrated in Figs. 2 (a) and (b), respectively. It implies that we can predict the electrical failure yield of one system if a stress condition of the other system is prepared. For example, a number of AM29SL800DT/DB with TSOP048 units is tested at 1500 V by JEDEC system. Regarding the electrical failure yield of this JEDEC stress level in Fig. 2 (a), it is 33.33%. Then, we can convert the stress level to around approximately 1100 V in ESDA system by the linear relationship. That means the electrical failure yield of these samples at 1100 V ESDA is approximately 33.33%.

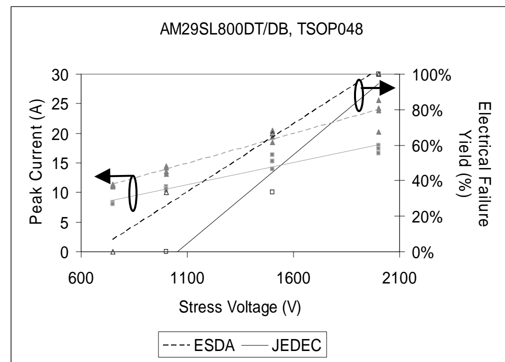




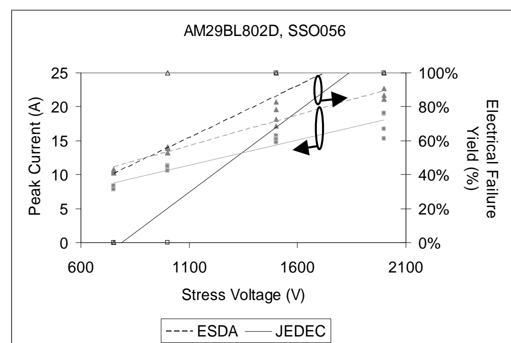
(a)

(b)

Fig.1 (a) 1st peak current and (b) stress condition relations between ESDA and JEDEC systems



(a)



(b)

Fig. 2 Relation of electrical failure yield and stress voltage compared with the peak current in ESDA and JEDEC systems, products: (a) AM29SL800DT/DB, TSOP048 and

(b) AM29BL802D, SSO056

4 CONCLUSIONS

The ESD-CDM standards released by ESDA and JEDEC are commonly used to verify the component-level ESD robustness of IC products by the semiconductor industry. With their specifications, major instrumental discrepancies and details have been studied. The relationship between peak currents and stress conditions of both ESDA and JEDEC systems has been presented and discussed. The results of discharge current, rise time and full width at half maximum show that ESDA standard provides a test system with a higher inductance and a more severe CDM stress. What to point out is that, peak currents have been reasonable analyzed and proposed to represent a relation of the stress condition. A linear relationship of stress conditions between these two standards has been observed by waveform verification. Therefore, we can estimate an electrical failure yield of each system if a stress condition of the other system is provided.

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